Delay Line

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In my discussion with John Anderson, the following recommendations for implementation of delay lines were discussed:

1) Used Silicon Delay lines
2) Configure FPGA as D flip-flops.
3) Configure FPGA to detect the rising and falling edge of the signal and to re-create it with the desired delay.

Silicon Delay Line

Using silicon delay is a very simple method to create the necessary delay. The advantage of using this method is as follows:

1) Very simple to implement.
2) They come with buffer inputs, outputs and therefore impedance matching is not a problem.
3) Easy to adjust individual boards for variation in delays.

Disadvantage

1) Takes up a lot of real-estate.
2) Board will be design specific.

Configuring FPGA as D flip-flops

Using FPGA as D flip-flops is a very simple method to create the necessary delay. The advantage of using this method is as follows:

1) Very simple to implement
2) Delay of signal is simply the number of flip-flop plus the inherent delay cause by the flip-flops.

Disadvantage

1) Needs large number of D flips-flops to be programmed
2) Finding the right clock signal
3) There maybe unwanted changes in signal parameters.

Configuring FPGA to detect the rising and falling edge of the signal and to re-create it with the desired delay.

Configure FPGA to detect the rising and falling edge of the signal and to re-create it with the desired delay needs a more program intensive algorithm. The advantage of using this method is as follows:

1) Utilizes less flip-flops
2) Signals should be clones of the original.

Disadvantage

1) Finding the right clock signal.

AFT signals.

Looking at the signals at SASEQ at the test bench, Micheal Matulik and I measured the signals needed for the AFT to give us an idea of range of signals. It was observed that **smallest signal need to be delayed is the Digitize Differential Clock in the SVX which has a period of approximately 18ns with a pulse width of 8ns.**

This small signal is a problem for our present FPG design because inorder to reproduce an 8ns pulse we need a clock that is atleast 4ns wide. This means that the sampling frequency of the FPGA needs to be greater than 250MHz.

The DS1013 silicon delay line was recommended the but its minimum width requirement is 10ns.